PCT/IB05/50654

INVESTOR IN PEOPLE

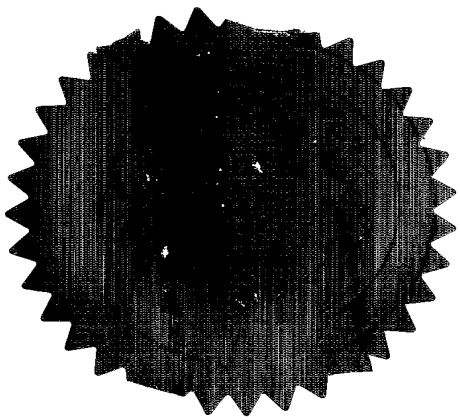
The Patent Office
Concept House
Cardiff Road
Newport
South Wales
NP10 8QQ

I, the undersigned, being an officer duly authorised in accordance with Section 74(1) and (4) of the Deregulation & Contracting Out Act 1994, to sign and issue certificates on behalf of the Comptroller-General, hereby certify that annexed hereto is a true copy of the documents as originally filed in connection with the patent application identified therein.

In accordance with the Patents (Companies Re-registration) Rules 1982, if a company named in this certificate and any accompanying documents has re-registered under the Companies Act 1980 with the same name as that with which it was registered immediately before re-registration save for the substitution as, or inclusion as, the last part of the name of the words "public limited company" or their equivalents in Welsh, references to the name of the company in this certificate and any accompanying documents shall be treated as references to the name with which it is so re-registered.

In accordance with the rules, the words "public limited company" may be replaced by p.l.c., plc, P.L.C. or PLC.

Re-registration under the Companies Act does not constitute a new legal entity but merely subjects the company to certain additional company law rules.



Signed

Dated 14 January 2005

PRIORITY DOCUMENT
SUBMITTED OR TRANSMITTED IN COMPLIANCE WITH RULE 17.1(a) OR (b)

Patents Form 1/77

[redacted]ts Act 1977
16)

The **Patent Office**

1/77

THE PATENT OFFICE
A
- 3 MAR 2004
NEWPORT

Request for grant of a patent
(See notes on the back of this form. You can also get an explanatory leaflet from the Patent Office to help you fill in this form)

The Patent Office

Cardiff Road
Newport
Gwent NP10 8QQ

1. Your reference — 0 3 MAR 2004 — PHGB040053GBP

2. Patent application number
(The Patent Office will fill in this) 0404751.0

3. Full name, address and postcode of the or of each applicant (*underline all surnames*)

KONINKLIJKE PHILIPS ELECTRONICS N.V.
GROENEWOUDSEWEG 1
5621 BA EINDHOVEN
THE NETHERLANDS

Patents ADP Number (*if you know it*) 07419294001

If the applicant is a corporate body, give the country/state of its incorporation: THE NETHERLANDS

4. Title of the invention: TRENCH FIELD EFFECT TRANSISTOR AND METHOD OF MAKING IT

5. Name of your agent (*if you have one*)

"Address for service" in the United Kingdom to which all correspondence should be sent (*including the postcode*)

Philips Intellectual Property & Standards
Cross Oak Lane
Redhill
Surrey RH1 5HA

Patents ADP number (*if you know it*) 08359655001

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and (*if you know it*) the or each application number

Country	Priority Application number	Date of filing

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

Number of earlier application	Date of filing (*day/month/year*)

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? (*Answer "Yes" if:*
   a) *any applicant named in part 3 is not an inventor, or*
   b) *there is an inventor who is not named as an applicant, or*
   c) *any named applicant is a corporate body.*
   See note (d))

YES

Patents Form 1/77

9. Enter the number of sheets for any of the following items you are filing with this form.
Do not count copies of the same document.

Continuation sheets of this form	
Description	8
Claims(s)	3 CF
Abstract	1
Drawings	4 only

10. If you are also filing any of the following, state how many against each item:

Priority Documents	
Translations of priority documents	
Statement of inventorship and right to grant of a patent (*Patents Form 7/77*)	
Request for preliminary examination and search (*Patents Form 9/77*)	
Request for substantive examination (*Patents Form 10/77*)	
Any other documents (*Please specify*)	

11. I/We request the grant of a patent on the basis of this application.

Signature D. J. Sharrock Date 2 MAR 04

12. Name and daytime telephone number of person to contact in the United Kingdom 01293 815399 D. J. SHARROCK

Warning

After an application for a patent has been filed, the Comptroller of the Patent Office will consider whether publication or communication of the invention should be prohibited or restricted under Section 22 of the Patents Act 1977. You will be informed if it is necessary to prohibit or restrict your invention in this way. Furthermore, if you live in the United Kingdom, Section 23 of the Patents Act 1977 stops you from applying for a patent abroad without first getting written permission from the Patent Office unless an application has been filed at least 6 weeks beforehand in the United Kingdom for a patent for the same invention and either no direction prohibiting publication or communication has been given, or any such direction has been revoked.

Notes

a) If you need help to fill in this form or you have any questions, please contact the Patent Office on 0645 500505.

b) Write your answers in capital letters using black ink or you may type them.

c) If there is not enough space for all the relevant details on any part of this form, please continue on a separate sheet of paper and write "see continuation sheet" in the relevant part(s). Any continuation sheet should be attached to this form.

d) If you have answered "Yes" Patents Form 7/77 will need to be filed.

e) Once you have filled in the form you must remember to sign and date it.

f) For details of the fee and ways to pay please contact the Patent Office.

DESCRIPTION

TRENCH FIELD EFFECT TRANSISTOR AND METHOD OF MAKING IT

The invention relates to a trench field effect transistor (trench-FET) and to a method of making it.

An example of a prior art trench semiconductor structure is illustrated in Figure 1. An n-type drain layer 4 is provided over an n+ substrate 2, and a p-type body layer 20 is provided on the drain layer 4. A trench 6 extends through the body layer 20 as far as the drain layer 4, and includes a conductive gate 10 insulated from the body layer by a gate insulator 9. N+ source diffusions 14 are provided adjacent to the trench. Gate electrode 26 connects to the gate 10, source electrode 22 connects to the source 14 and body 20 and drain electrode 24 connects to the substrate 2.

In use, a voltage is applied to the gate electrode 26 to control a channel extending in the body layer 20 adjacent to the trench 6 between the source 14 and drain 4.

A reduction of the cell pitch, i.e. the distance between adjacent cells, of a trench-FET is generally desirable, as the lower the cell pitch the greater the channel width for a fixed area of silicon. Thus, the specific on-resistance, i.e. the resistance of the FET when switched on per unit area, may be reduced by lowering the cell pitch.

The reduction in cell pitch requires a reduction in the width of either the trench region, containing the gate, and/or the mesa region, i.e. the region with implanted source and body regions.

Recently, a reduction in mesa width has been obtained by a blanket source implantation. In the schematic of Figure 1 above, both the body region and the source region are exposed at the first major surface. In the technique of blanket source implantation, the source region is implanted over the whole of the mesa at the first major surface leaving the body below the source

region. Since it is no longer necessary to have both source and body at the first major surface of the mesa, the mesa width can be reduced.

The downside of this approach is that it is still necessary to contact the body. This is achieved by a moat etch through the source region to the body region and a highly doped contact implant in the body region to provide a contact to the body region at the base of the moat etch. If the contact implant were to diffuse to the channel the device would become hard to turn on. It is therefore necessary that the moat is spaced away from the channel by some distance. Thus, there are limits to how far the cell pitch can be reduced using this approach.

There thus remains a need to reduce the cell pitch of trench-FET structures.

According to the invention, there is provided a trench field effect transistor (trench-FET) comprising:

a semiconductor body having opposed first and second major surfaces;

a source metallisation at the first major surface;

source contact regions of semiconductor doped to have a first conductivity type at the first major surface in contact with the source metallisation;

body contact regions of semiconductor doped to have a second conductivity type opposite to the first conductivity type at the first major surface in contact with the source metallisation;

a drain region of first conductivity type under the first major surface;

a drain contact connected to the drain region; and

insulated gates including a conductive gate in an insulated trench for controlling current flow between the source contact region and the drain region through mesa regions between the insulated gates,

wherein the source contact regions and base contact regions alternate laterally across the first major surface, with the source contact regions arranged in the insulated trench above the insulated gate.

By providing the source regions above the insulated gate the cell pitch can be substantially reduced.

For example, in preferred embodiments of the invention the cell pitch can be reduced below 1 micron. Pitches below 0.5 micron may be achieved.

Preferably, the mesa regions comprise doped body regions of semiconductor doped to have the second conductivity type extending under the body contact region to the drain region, the doped body regions having a lower doping density than the body contact regions.

The source contact region may extend to a greater depth than the base contact region so that the source contact region is in direct contact with the doped body region under the body contact region. This means that current can flow from the source contact region through the doped body region past the insulated gate to the drain region.

In embodiments, the first conductivity type is n-type and the second conductivity type p-type, the p-type doping of the body contact region being above $5x10^{18}$ cm^{-3}, the p-type doping of the body region being in the range 10^{17} cm^{-3} to 10^{18} cm^{-3}, and the doping of the n-type source contact region being above 10^{19} cm^{-3}.

The drain region may include a drift region of lower doping above a highly doped drain region of higher doping than the drift region, both drain and drift regions being of the first conductivity type.

The doping in the drift region may be below 10^{17} cm^{-3}, preferably below $5x10^{16}$ cm^{-3}, although the exact value will depend on the properties required and especially the breakdown voltage. The doping in the highly doped drain region may above 10^{18} cm^{-3}, and is preferably highly conducting with a doping density above 10^{19} cm^{-3}, to reduce the overall resistance of the device.

The drift region may be formed as an epitaxial layer on a highly doped substrate forming the highly doped drain region. Alternatively the drift region and/or drain regions may be formed by implanting dopants.

It is not necessary that the source contact regions are confined to the trenches and the source contact regions may extend laterally outside the confines of the trenches as well as above the insulated gate so that the width

of the body contact regions between the source contact regions is narrower than the width of the mesa regions between the trenches. This can reduce the effects of current crowding at the top corner of the insulated gates. Such source contact regions extending outside the confines of the trench may be made simply by annealing the structure to allow the dopants in the source contact region to diffuse outwards, so such a structure is not difficult to manufacture.

In another aspect, the invention relates to a method of manufacturing a trench-FET, including the steps of:

providing a semiconductor having opposed first and second major surfaces doped to be of first conductivity type to form a drain region;

implanting a body contact region at the first major surface of semiconductor doped to be of a second conductivity type opposite to the first conductivity type;

forming trenches laterally across the first major surface alternating laterally with the body contact regions, the trenches extending below the body contact regions defining mesa regions below the body contact regions between the trenches;

forming insulated gates in the trenches;

depositing source regions of semiconductor doped to be of the first conductivity type in the trenches above the insulated gates; and

depositing a source metallisation at the first major surface contacting the source regions and the body contact regions.

It is of particular benefit that the body contact region may be formed by implantation at the whole of the first major surface since the unwanted doping will be removed when forming the trenches.

The method may include the step of implanting body regions of second conductivity type to a first depth greater than the depth of the source contact regions wherein the body contact implantation is carried out to a second depth less than the depth of the source contact regions so that the body contact region lies above the body regions in the finished FET.

The step of forming insulating gates in the trenches may include the steps of forming insulator on the sidewalls and base of the trenches, forming gate conductor in the trenches to a depth below the top of the trenches and forming gate-source insulator in the trenches above the gate conductor.

For a better understanding of the invention, embodiments will be described with reference to the accompanying drawings in which:

Figure 1 illustrates a prior art trench-FET;

Figure 2 illustrates a first step in a process according to a first embodiment of the invention;

Figure 3 illustrates the trench FET according to the first embodiment;

Figure 4 shows a simulated doping profile for the first embodiment; and

Figure 5 shows the current with the device switched off as a function of source-drain voltage; and

Figure 6 shows simulated specific Rdson values for the first embodiment.

Note that the Figures are schematic and not to scale and that like or similar components are shown with the same reference numeral in different Figures.

The manufacture of the device is largely conventional except for the filled trenches. Figure 2 illustrates a step in the manufacture of one of these trenches.

To form the trenches 6, a mask, conveniently of photoresist, is patterned and the epilayer 4 etched to define trenches 6 extending through epilayer 4 towards substrate 2. Insulator is formed on the sidewalls 9 and base 8 of the trenches 6 and gate polysilicon 10 deposited in the trenches 6 and doped. Next, the gate polysilicon 10 is etched down below the top of the substrate to the required depth in the trench. The mask is then removed.

A nitride layer 30 is deposited over the whole surface to a thickness of 30nm to 100nm. Next, a spacer etch is performed which removes the nitride

from all surfaces except the sidewalls arriving at the structure shown in Figure 2.

A wet oxidation step is carried out to grow oxide on the polysilicon gate region.

Next, hot phosphoric acid is used to etch away the nitride. Phosphoric acid selectively etches nitride and does not etch oxide.

Polysilicon is deposited in the top of the trench, and doped with arsenic to a doping density of $1x10^{21}$ cm^{-3} to form source regions 14.

Subsequent processing follows standard processes to arrive at the finished structure of Figure 3.

It is a particular benefit of the method that the implants to form both the body region 20 and the body contact region 18 can be made over the whole of the surface unlike the contact to the body formed in a prior art structure using a moat etch, in which prior art structure the body contact implant needs to be kept away from the channel.

In the finished device, as shown in Figure 3, highly doped n+ substrate 2 forms the drain and epilayer 4 forms the drift region. The epi-layer is doped $3x10^{16}$ cm^{-3} n-type.

Trenches 6 extend from the first major surface into epilayer 4. The trenches 6 include a thick trench base insulator 8 on the base of the trench, gate insulator 9 on the sidewalls of the trench 6, a conductive gate electrode 10, in the example of doped polysilicon filling the trench, and a gate-source insulator 12 above the gate electrode 10. Source region 14 of n+-doped semiconductor fills the top of the trench to a depth of 0.3 μm.

Mesa region 16 between the trenches includes a body contact region 18 at the top surface heavily doped p+, in the example $2x10^{19}$ cm^{-3}, extending to a depth of 0.25 micron. Below the body contact region 18 is the body region 20, extending to meet the drain region 4 between the trenches. The slightly shallower depth of the body contact region 18 than the source region 14 helps reduce the current crowding at the top corner of the insulated gate 10.

Source contact 22 extends along the top of the first major surface contacting the source regions 14 and body contact regions 18. The source

regions 14 and body contact regions 18 are arranged in stripes across the surface extending in the direction into the paper in Figure 3.

A drain contact 24 contacts the rear of the substrate 2. As will be appreciated, in alternative embodiments a highly doped epi-layer 4 can be used and contact made directly to the epilayer.

Figure 4 shows the doping profile in the mesa region measured from the top surface.

Figure 5 shows the current with the device switched off with 1.5V applied to the gate as a function of applied drain-source voltage. Breakdown at 29.5 V can be clearly seen.

Figure 6 shows the specific on-resistance Rdson with the device turned on at a number of gate voltages. With a gate voltage of 10V the specific on resistance is 6.2mΩ.mm^2 from the device of which the substrate makes a contribution of 3.6mΩ.mm^2. Thus the device has a very low specific on-resistance.

This is achieved using a very simple structure which importantly is easy to manufacture with very small cell pitch.

The skilled person will appreciate that a number of modifications may be made to the embodiments without departing from the scope of the invention. In particular, the n- and p- type regions may be interchanged.

The invention is not just applicable to silicon as the semiconductor but may be applied in any suitable semiconductor including for example GaAs. Further, the device is of simple form and may be used not merely on a single crystal substrate but also as part of thin film transistors.

From reading the present disclosure, other variations and modifications will be apparent to persons skilled in the art. Such variations and modifications may involve equivalent and other features which are already known in the design, manufacture and use of more boilerplate and which may be used in addition to or instead of features described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of disclosure also includes any novel feature or any novel combination of features disclosed herein either explicitly or implicitly

or any generalisation thereof, whether or not it mitigates any or all of the same technical problems as does the present invention. The applicants hereby give notice that new claims may be formulated to any such features and/or combinations of such features during the prosecution of the present application or of any further applications derived therefrom.

CLAIMS

1. A trench field effect transistor (trench-FET) comprising:

a semiconductor body having opposed first and second major surfaces;

a source metallisation (22) at the first major surface;

source contact regions (14) of semiconductor doped to have a first conductivity type at the first major surface in contact with the source metallisation (22);

body contact regions (18) of semiconductor doped to have a second conductivity type opposite to the first conductivity type at the first major surface in contact with the source metallisation;

a drain region (2,4) of first conductivity type under the first major surface;

a drain contact (24) connected to the drain region; and

insulated gates (10) including a conductive gate (10) in an insulated trench (6) for controlling current flow between the source contact region (14) and the drain region (2,4) through mesa regions (16) between the insulated gates,

wherein the source contact regions (14) and base contact regions (18) alternate laterally across the first major surface, with the source contact region arranged in the insulated trench (6) above the insulated gate.

2. A trench-FET according to claim 1 wherein the mesa regions comprise doped body regions (20) of semiconductor doped to have the second conductivity type extending under the body contact regions (18) to the drain region (2,4), the doped body regions (20) having a lower doping density than the body contact regions.

3. A trench-FET according to claim 2 wherein the source contact regions (14) extend to a greater depth than the base contact regions (18) so that the source contact regions (14) are in direct contact with the doped body regions (20) under the body contact regions (18) so that current can flow from

the source contact regions (14) through the doped body regions (20) past the insulated gate (10) to the drain regions (2,4).

4. A trench-FET according to claim 2 or 3 wherein the first conductivity type is n-type and the second conductivity type p-type, the p-type doping of the body contact region being above $5x10^{18}$ cm^{-3}, the p-type doping of the body region being in the range 10^{17} cm^{-3} to 10^{18} cm^{-3}, and the doping of the n-type source contact region being above 10^{19} cm^{-3}.

5. A trench-FET according to any preceding claim wherein the drain regions include a drift region (4) of lower doping above a highly doped drain region (2) of higher doping than the drift region, both drain and drift regions being of the first conductivity type.

6. A trench-FET according to claim 5 wherein the doping in the drift region (4) is below 10^{17} cm^{-3} and the doping in the highly doped drain region (2) is above 10^{18} cm^{-3}.

7. A trench-FET according to any preceding claim wherein the source contact regions (14) extend laterally outside the confines of the trenches (6) as well as above the insulated gate (10) so that the width of the body contact regions (22) between the source contact regions (14) is narrower than the width of the mesa regions between the trenches.

8. A method of manufacturing a trench-FET, including the steps of:

providing a semiconductor body (2,4) having opposed first and second major surfaces doped to be of first conductivity type to form a drain region;

implanting a body contact region (18) at the first major surface of semiconductor doped to be of a second conductivity type opposite to the first conductivity type;

forming trenches (6) laterally across the first major surface alternating laterally with the body contact regions (18), the trenches extending below the

body contact regions (18) defining mesa regions below the body contact regions (18) between the trenches (6);

forming insulated gates (10) in the trenches (6);

depositing source regions (14) of semiconductor doped to be of the first conductivity type in the trenches (6) above the insulated gates (10); and

depositing a source metallisation (22) at the first major surface contacting the source regions (14) and the body contact regions (18).

9. A method according to claim 8 further comprising the step of implanting body regions (20) of second conductivity type to a first depth greater than the depth of the source contact regions (14) wherein the body contact implantation (18) is carried out to a second depth less than the first depth.

10. A method according to claim 8 or 9 wherein the step of forming insulating gates (10) in the trenches includes the steps of forming insulator (8,9) on the sidewalls and base of the trenches (6), forming gate conductor (10) in the trenches (6) to a depth below the top of the trenches and forming gate-source insulator (12) in the trenches above the gate conductor (10).

11. A trench-FET substantially as described herein with reference to figures 2 to 6 of the accompanying Drawings.

12. A method of manufacturing a trench-FET substantially as described herein with reference to figures 2 to 6 of the accompanying Drawings.

ABSTRACT

TRENCH FIELD EFFECT TRANSISTOR AND METHOD OF MAKING IT

A trench-FET has source regions arranged above insulated gates 10 in trenches 6. Body region 20 of opposite conductivity type is arranged between the trenches 6 and body contact region 18 is arranged above the body region 20. Source contact metallisation 22 contacts the source 14 and body contact region 20. In this way a small cell pitch can be achieved.

[Fig 3]

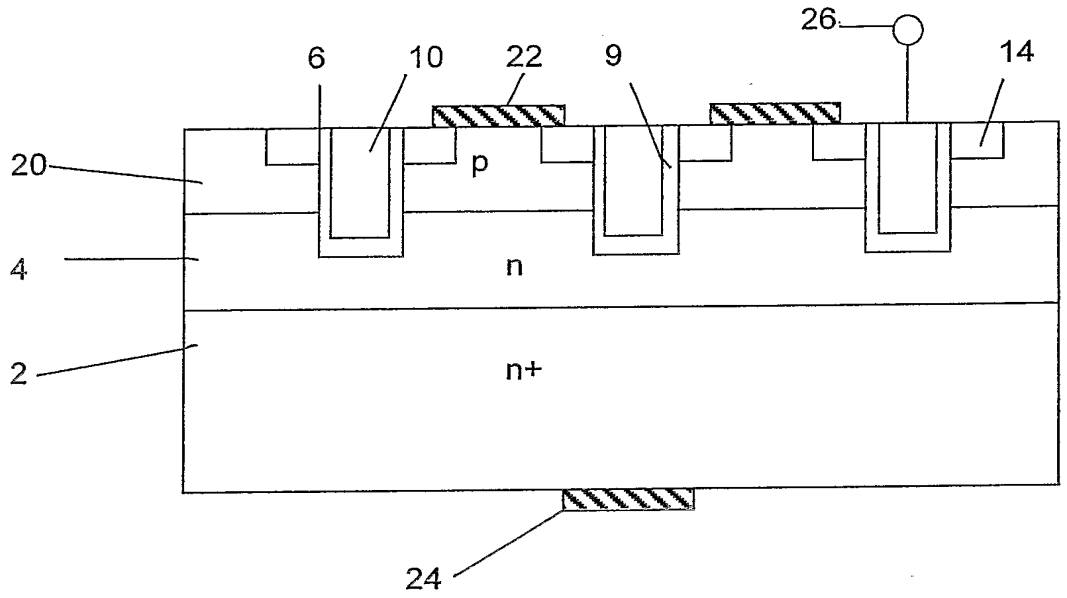
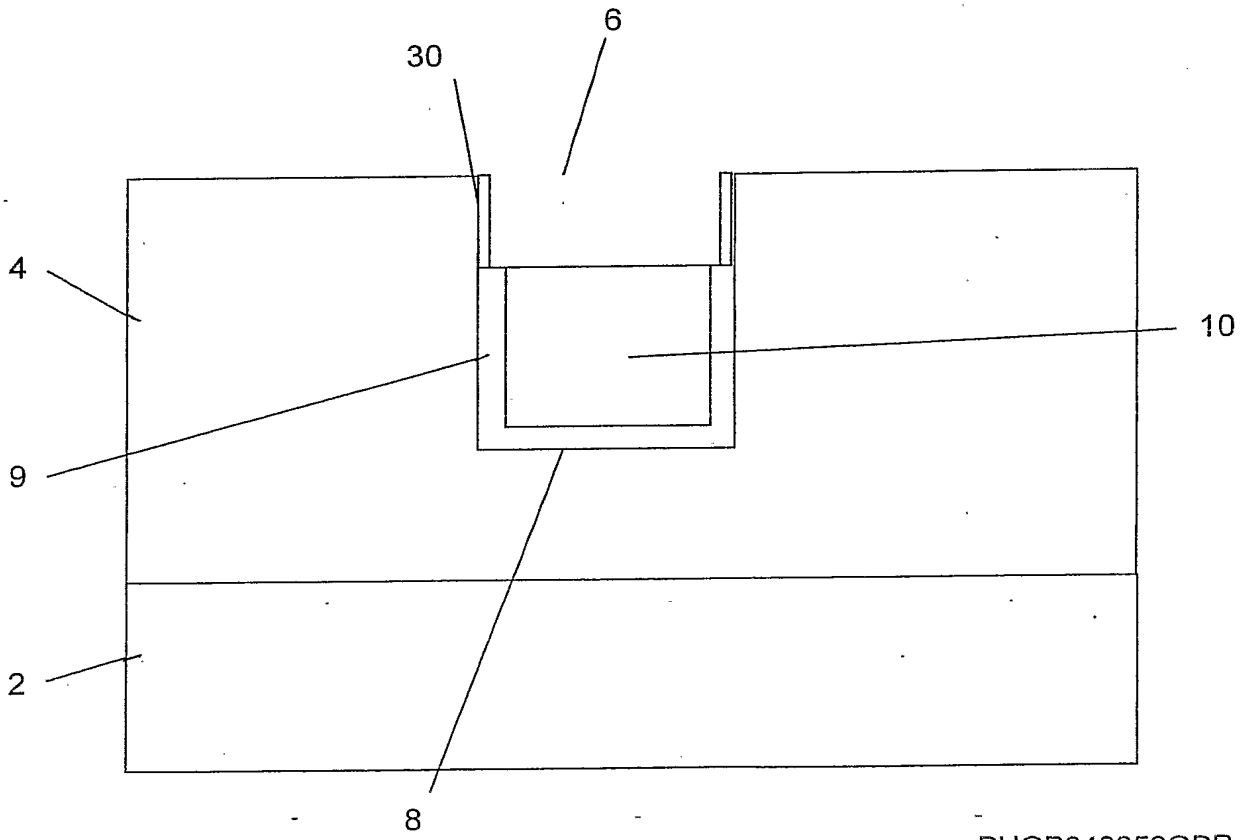


Fig. 1



PHGB040053GBP

Fig. 2

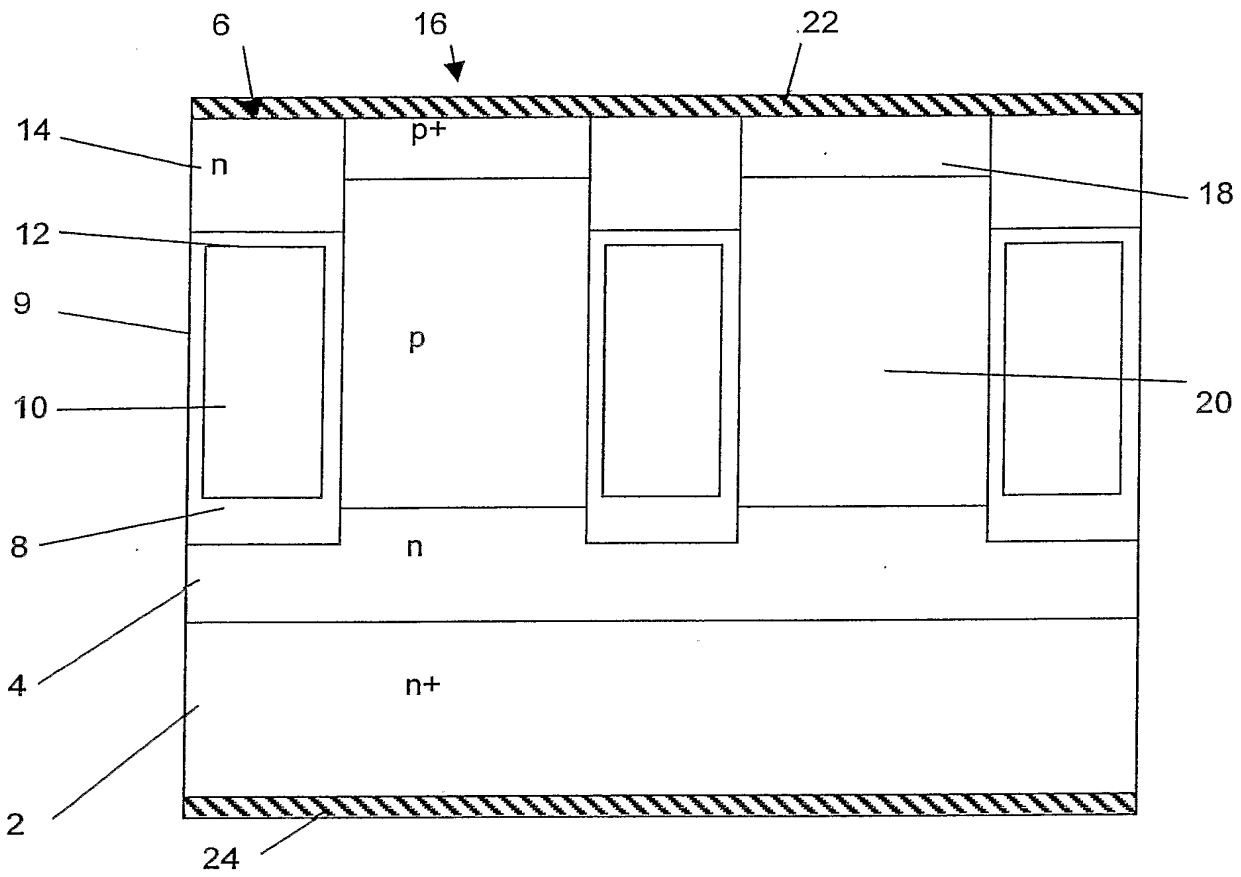


Fig. 3

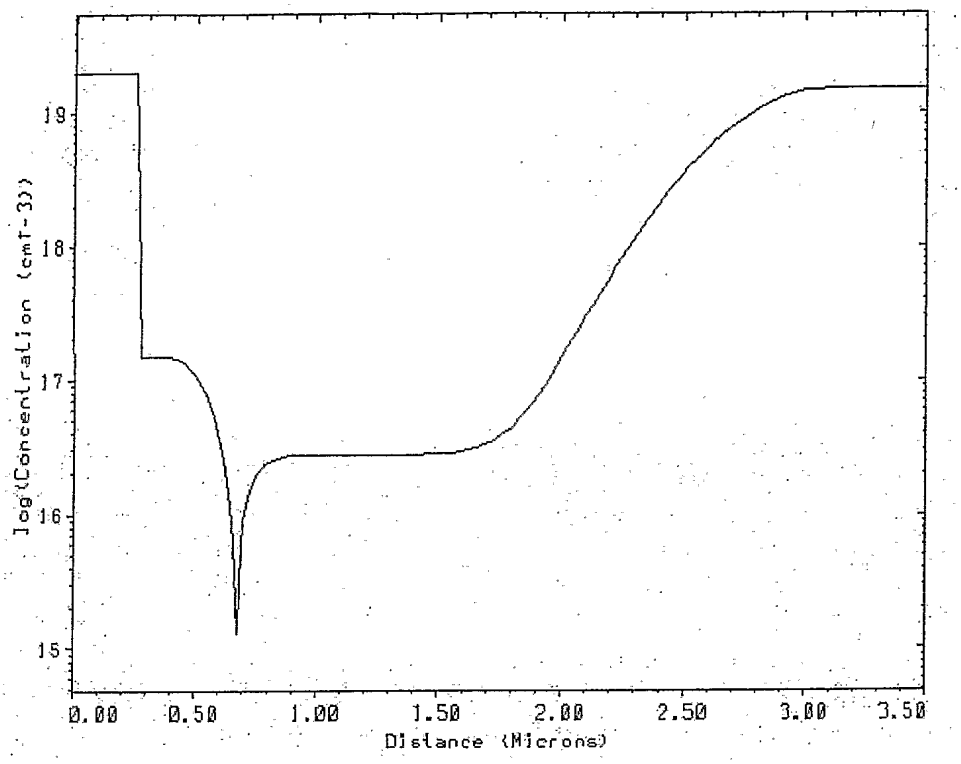

log(Concentration (cm^-3))
19
18
17
16
15
0.00
0.50
1.00
1.50
2.00
2.50
3.00
3.50
Distance (Microns)

Fig.4

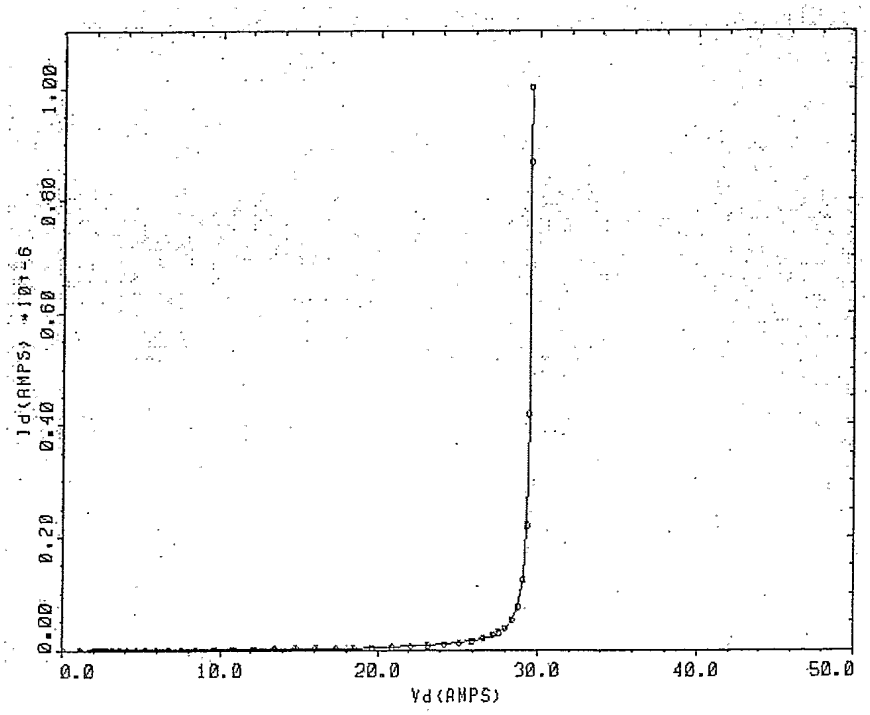

Id(AMPS) * 10^-6
1.00
0.80
0.60
0.40
0.20
0.00
0.0
10.0
20.0
30.0
40.0
50.0
Vd(AMPS)

Fig.5

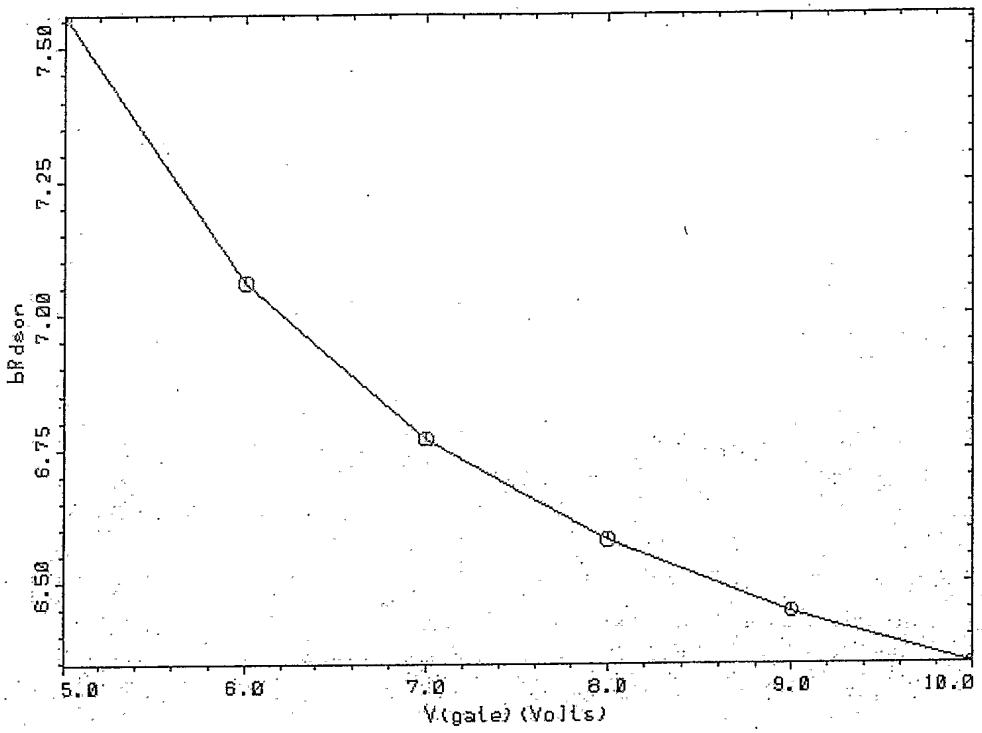


Fig. 6